THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WILLIAM M. PETERSON
and
SIDNEY C. GARRISON, III

Appeal No. 95-2782
Application 07/844,328[1]

ON BRIEF

Before HAIRSTON, KRASS and JERRY SMITH, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

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[1] Application for patent filed March 2, 1992.

This is an appeal from the final rejection of claims 2 through 17. In an Amendment After Final (paper number 5), claims 6 and 17 were amended.

The disclosed invention relates to a method and apparatus for performing bi-directional signal transformations through a network of weighting elements in a neural network.

Claims 15 and 17 are illustrative of the claimed invention, and they read as follows:

15. A method of performing bi-directional signal transformations through a network of weighting elements, comprising the steps of:

processing elements of an input signal vector in a forward direction through a plurality of synapses respectively in each of a plurality of neurons for providing an output signal from each of said plurality of neurons;

feeding back a first one of said output signals from said plurality of neurons through a first synapse having a predetermined positive value to increase said first one of said output signals; and

feeding back a second one of said output signals from said plurality of neurons through a second synapse having a predetermined negative value to decrease said first one of said output signals where a resulting said first one of said output signals is reverse processed through said plurality of synapses.

17. A neural network, comprising:

a plurality of neurons each having first I/O terminals and second I/O terminals, said first I/O terminals respectively receiving elements of an input signal vector, said plurality of neurons each including a plurality of bi-directional synapses each with a first terminal coupled for receiving one of said elements of said input signal vector and a second terminal coupled to said second I/O terminals such that a first one of said second I/O terminals provides an output signal in response to said input signal vector; and

circuit means coupled to said second I/O terminals of said plurality of neurons for monitoring said output signals thereof to select at least one of said output signals of said plurality of neurons having bi-directional synapses with a closest match to said input signal vector, said circuit means providing an output signal to a second one of said second I/O terminals of said selected at least one of said plurality of neurons for processing in a reverse direction through said selected at least one of said plurality of neurons and providing an output signal vector at said first I/O terminals.

The reference relied on by the examiner is:

Peterson et al. (Peterson) 5,065,040 Nov. 12, 1991

Claims 2 through 17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Peterson.

Reference is made to the brief and the answer for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the 35 U.S.C. § 102(b) rejection of claims 2 through 17.

Appellants indicate at pages 5 and 6 of the specification that the input signal vectors presented at input terminals 20 through 26 to the neurons 12 through 18 may initially pass through sample and hold circuits and switchable driver circuits before passing through the network of neurons. According to appellants, such neural network structure is disclosed by the reference to Peterson. The referenced portion of the specification also makes clear that the neurons 12 through 18 must be capable of bi-directional signal transformation as described in the Peterson reference. Thus, appellants have acknowledged that bi-directional signal transformation through a neural network that includes sample and hold circuits and switchable driver circuits is well known in the art.

The bi-directional signal flow through the neural network 70 in Figure 4 of Peterson is controlled by a switch control circuit

154 that provides first, second, third and fourth switch control signals for controlling the operation of switchable driver circuits 74 through 84, and sample and hold circuits 92 through 96 and 110 through 114. Peterson explains (column 7, line 20 through column 8, line 21) that the input signal vector is sent back and forth through the matrix of synapses in the weighting matrix 72 of the neural network 70 to improve the input signal. Although the switch control circuit 154 controls the selection of an output signal at the sample and hold circuits to route back through the bi-directional neural network 70, the reference to Peterson never explains how or on what basis the switch control circuit 154 makes such a selection. Figures 8 and 9 of Peterson illustrate two different synapses for use in the Figure 4 matrix of synapses. The two different synapses use multipliers and a learning circuit 198 to apply weights to the signals passing therethrough.

Turning first to claims 6 and 17, we find that the neural network in the reference to Peterson operates in substantially the same manner as the disclosed and claimed neural network,

except for the step of monitoring the signals to select at least one of the output signals from the plurality of neurons having a "greatest activity level" (claim 6), and the circuit means to make a selection of at least one of the output signals from the plurality of neurons based upon a "closest match to said input signal vector" (claim 17). As indicated supra, the switch control circuit 154 in the reference to Peterson does not select a signal for reverse or any other bi-directional processing based upon "greatest activity level" of the signal or because the signal is the "closest match to said input signal vector." The 35 U.S.C. § 102(b) rejection of claims 6 and 17 and the claims that depend therefrom is reversed because each and every limitation of these claims is not found in the reference to Peterson. See RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.), cert. dismissed, 468 U.S. 1228 (1984).

Turning next to claims 8 and 15, the two different synapses in Figures 8 and 9 of Peterson use multipliers and a learning circuit 198 to weight the signals passing therethrough. The

learning circuit 198 is described (column 10, lines 54 through 60) as providing an "adjustable reference signal." Although a case can be made that a multiplier may add a "positive value" to a signal passing through the synapse, we fail to see how that same multiplier can add a "negative value" to the signal. The examiner's reasoning certainly does not shed any light on this subject. Inasmuch as each and every limitation of claims 8 and 15 and the claims that depend therefrom is not found in the reference to Peterson, we will reverse the 35 U.S.C. §102(b) rejection of these claims.

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DECISION

The decision of the examiner rejecting claims 2 through 17 under 35 U.S.C. § 102(b) is reversed.

REVERSED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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ERROL A. KRASS) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
) INTERFERENCES
JERRY SMITH)
Administrative Patent Judge)

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